Remarks:

Reconsideration of the application is requested.

Claims 1-10 remain in the application.

In item 3 on page 2 of the above-identified Office Action, claims 1 and 3-7 have been rejected as being anticipated by Fang (U.S. Patent No. 6,316,293) under 35 U.S.C. § 102(e).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and, therefore, the claims have not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a method for fabricating embedded nonvolatile semiconductor memory cells, which comprises the steps of:

providing a substrate divided into a high-voltage region, a memory region and a logic region;

forming a first insulating layer on the substrate in the high-voltage region, the memory region and the logic region;

removing the first insulating layer in the memory region;

forming a second insulating layer in the high-voltage region, the memory region and the logic region;

forming a charge storing layer in the high-voltage region, the memory region and the logic region;

patterning the charge-storing layer in the memory region;

forming a third insulating layer in the high-voltage region, the memory region and the logic region;

removing the first to third insulating layers and also the charge-storing layer in the logic region;

forming a fourth insulating layer in the high-voltage region, the memory region and the logic region; and

forming and patterning a conductive control layer in the high-voltage region, the memory region and the logic region. (emphasis added)

Thus, according to the present invention, there is provided a method for fabricating embedded nonvolatile semiconductor

memory cells. The method includes the steps of providing a substrate divided into a high-voltage region, a memory region and a logic region; forming a first insulating layer on the substrate in the high-voltage region, the memory region and the logic region; removing the first insulating layer in the memory region; forming a second insulating layer in the high-voltage region, the memory region and the logic region; forming a charge storing layer in the high-voltage region, the memory region and the logic region; patterning the charge-storing layer in the memory region; forming a third insulating layer in the high-voltage region, the memory region and the logic region; removing the first to third insulating layers and also the charge-storing layer in the logic region; forming a fourth insulating layer in the high-voltage region, the memory region and the logic region; and forming and patterning a conductive control layer in the high-voltage region, the memory region and the logic region.

It is preferable for the charge-storing layer to be patterned and then the third insulating layer to be formed in a whole-area manner thereon. As a result, improved sidewall isolation is produced for the charge-storing layer elements and the charge retention times can be improved.

The charge-storing layer contains an electrically conductive or an electrically nonconductive layer, which enables

different types of nonvolatile semiconductor cells to be provided.

An ONO layer sequence is preferably formed as the third insulating layer. This layer sequence has outstanding coupling properties combined with ease of fabrication.

The Fang reference discloses a method of forming NAND-type flash memory devices. The disclosed method forms a core memory cell and periphery transistors (both high and low voltage). Various layers are formed on a substrate 104. A photoresist mask 103 is removed and oxide layer 108 is formed over the surface of the device. A tunnel oxide mask is formed to define an area 114 within the core region 105 in which the tunnel oxide for the core memory cells is formed. The layer 114 is removed on the area 114, but not in the peripheral regions 116, 118. A second layer 119 is only formed over the region 114, not the high voltage, memory and logic regions as claimed. A third insulating layer 130 only overlies layer 122; it does not form in the high-voltage, memory, and logic regions as claimed; and there is no disclosure that the first second and third insulating layers and the charge-storing layer are removed from the logic region as recited in the claims. Nor is the fourth insulating layer 140, 142 formed in the high-voltage, memory, and logic regions as claimed, the

layers 140, 142 are only formed in the low and high voltage peripheral regions (see col. 7, lines 26-31).

Clearly, Fang does not show a method for fabricating embedded nonvolatile semiconductor memory cells, having the steps of "**forming a second insulating layer in the high-voltage region, the memory region and the logic region;** forming a charge storing layer in the high-voltage region, the memory region and the logic region; **forming a third insulating layer in the high-voltage region, the memory region and the logic region; removing the first to third insulating layers and also the charge-storing layer in the logic region; and forming a fourth insulating layer in the high-voltage region, the memory region and the logic region**", as recited in claim 1 of the instant application.

In item 12 on page 5 of the above-identified Office Action, claim 2 has been rejected as being unpatentable over Fang in view of Babayan (U.S. Patent No. 6,194,036) under 35 U.S.C. § 103(a).

The above discussion of Fang is applicable in the rejection of claim 2.

Babayan discloses deposition of coatings using an atmospheric pressure plasma jet. Babayan does not overcome the deficiencies of Fang.

In item 14 on page 6 of the above-identified Office Action, claim 8 has been rejected as being unpatentable over Fang in view of the Ghandi publication under 35 U.S.C. § 103(a).

The above discussion of Fang is applicable in the rejection of claim 8.

Ghandi discloses wet chemical etching fabrication principles. Ghandi does not overcome the deficiencies of Fang.

In item 16 on page 6 of the above-identified Office Action, claim 9 has been rejected as being unpatentable over Fang in view of the Ghandi publication under 35 U.S.C. § 103(a).

The above discussion of Fang is applicable in the rejection of claim 9.

Ghandi discloses wet etching chemical principles. Ghandi does not overcome the deficiencies of Fang.

In item 18 on page 7 of the above-identified Office Action, claim 10 has been rejected as being unpatentable over Fang in

view of Wu (U.S. Patent No. 6,261,964) under 35 U.S.C. § 103(a).

The above discussion of Fang is applicable in the rejection of claim 10.

Wu discloses a material removal process for forming a structure. Wu does not overcome the deficiencies of Fang.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims 2-10 are believed to be patentable as well, because they all are ultimately dependent on claim 1.

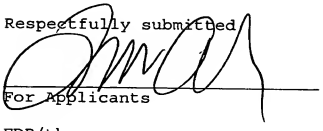
In view of the foregoing, reconsideration and allowance of claims 1-10 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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